

Confirmation No.8503

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	ROOZEBOOM <i>et al.</i>	Examiner:	Chen, David Z.
Serial No.:	10/560,717	Group Art Unit:	2815
Filed:	December 15, 2005	Docket No.:	NL040226US1 (NXPS.351PA)
Title:	ELECTRONIC DEVICE, ASSEMBLY AND METHODS OF MANUFACTURING AN ELECTRONIC DEVICE		

CORRECTION TO APPEAL BRIEF FILED ON FEBRUARY 18, 2010

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Dear Sir:

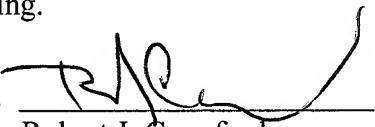
This Correction to Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in Response to the Office Communication dated March 12, 2010 and in support of the Notice of Appeal filed December 18, 2009 and in response to the rejections set forth in the Final Office Action dated September 18, 2009.

A correction is made to Section V, pages 2-3 of the Appeal Brief filed on February 18, 2010, regarding the description of independent claim 22. The correct claim to be described is claim 23. No other corrections or edits are intended in this paper. Entry of the attached Corrected Section V (pages 2-3) of the Appeal Brief is respectfully requested.

Appellant's Deposit Account No. 50-4019 (NL040226US1) was charged the requisite appeal brief fee. While no further charges should be necessary, authorization is given to charge the above account in support of this filing.

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I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-10 and 20-27 stand rejected and are presented for appeal. Claims 11-19 are cancelled. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated September 18, 2009.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to an electronic device comprising a semiconductor substrate having

a first side and a second side (*see, e.g.*, Figures 4a-4e, reference numbers 1 and 2). The electronic device having a vertical trench capacitor on the first side of the substrate (*see e.g.*, Figure 4b, reference number 21), the vertical trench capacitor including a plurality of trenches in which dielectric material is present between first and second conductive surfaces (*see, e.g.*, Figure 2c, reference 11 and page 11:15-19); and a vertical interconnect that extends through the substrate from the first side to the second side (*see, e.g.*, Fig. 2c, reference 30), the vertical interconnect being insulated from the substrate by dielectric material (*see, e.g.*, Fig. 2c, reference 30 and reference 11), the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor being common material formed from a single deposition layer (*see, e.g.*, Figure 2c and page 2: 30-34).

Commensurate with independent claim 23, an example embodiment of the present invention is directed to an electronic device comprising: a semiconductor substrate having a first side and a second side (*see, e.g.*, Figures 4a-4e, reference numbers 1 and 2); a plurality of trenches on the first side of the substrate (*see, e.g.*, Figure 4b, reference number 21), each of the trenches extending into the substrate from the first side (*see, e.g.*, *id.*); conductive material lining each of the trenches (*see, e.g.*, Figure 2b, reference 22 and page 10, 31-33); a vertical interconnect that extends through the substrate from the first side to the second side (*see, e.g.*, Figure 2c, reference 30), the vertical interconnect having walls (*see, e.g., id.*); a single deposition layer of dielectric material on the first and second sides of the substrate, on the conductive material lining each of the trenches, and on the walls of the vertical interconnect (*see, e.g.*, Figure 2c and page 2:30-34).